

# Optimum Characteristics of High Temperature Josephson Junctions for “Lumped” Array Applications\*

R.H. Ono and S.P. Benz

National Institute of Standards and Technology, Boulder, CO 80303, USA

**Abstract—** We present design criteria for arrays of Josephson junctions optimized for use in the Josephson digital-analog converter and for a THz oscillator. We will briefly analyze existing high temperature superconducting Josephson junction processes and describe possible implementation of a lumped array using electron-beam-damaged junctions and bilayer-SNS junctions.

## I. INTRODUCTION

This paper reviews the desired characteristics for high temperature superconducting (HTS) Josephson junctions for use in arrays. We will analyze the case of “lumped” (as opposed to “distributed”) systems where the circuit size is electrically small, that is, short compared to the wavelength of the radiation required.

Arrays of low- $T_c$  Josephson junctions are the basis for a number of applications within superconducting electronics including Josephson voltage standards, millimeter-wave oscillators, and microwave frequency clocks [1]. For useful power or voltage output, large numbers of junctions are typically required with small spreads in individual characteristics. For most system applications, the broadest possible bandwidth is desirable, as is rapid and simple tunability. Of course, the higher the operating temperature of the Josephson circuit, the simpler and cheaper are the system insertions.

High temperature superconducting (HTS) junctions may permit arrays that can operate in a compact and inexpensive cryogenic system. However, existing HTS junction technologies are still in their infancy, in particular with regards to spreads in junction critical currents. The individual characteristics of many HTS junctions are in some cases ideal for lumped array designs, and we will discuss this and examine some particular approaches to junction fabrication.

## II. REVIEW OF JUNCTION CHARACTERISTICS

HTS Josephson junctions typically are weak links that can be described by the Resistively-Shunted Junction (RSJ) model [2]. The important individual junction parameters are critical current  $I_c$ , normal resistance  $R_N$ ,

capacitance  $C_j$ , Josephson penetration depth  $\lambda_j$ , and the characteristic voltage  $V_c = I_c R_N$ . The spreads in these parameters over a large number of junctions should be small, as required by the operating margins of the array circuit. Practical issues of frequency source power and microwave or millimeter wave feed design must be taken into consideration. Operating temperature is a relatively unconstrained parameter, fundamentally related to thermal noise and stability of array operation. Higher temperature operation requires higher critical currents. In practice, these values are experimentally achieved in most HTS junction implementations. The following equations summarize the important junction and circuit characteristics:

$$V_j = \frac{h}{2e} f_0, \quad V_c = I_c R_N, \quad \Omega = \frac{f_0}{(2e/h)V_c}, \quad \beta_c = \frac{2e}{h} I_c R_N^2 C_j.$$

The ac Josephson effect predicts that currents in the junction will oscillate at a frequency  $f_0$  proportional to the time averaged voltage  $V_j$ ; this is the basis for the types of applications we are considering. The characteristic voltage of the junction sets a voltage (and hence frequency) scale for operation. The ratio of  $f_0$  to  $(2e/h)V_c$  is the dimensionless reduced frequency  $\Omega$ . The hysteresis parameter  $\beta_c$  should be much less than 1, requiring either a very small junction capacitance, external shunting to reduce junction resistance, or both. As we will see in the next section,  $I_c$  and  $R_N$  are chosen to maximize  $I_c$  and to set the product to approximately correspond to the frequency of interest.

## III. ARRAY REQUIREMENTS

Given the above general constraints, we now discuss the particular requirements imposed by our applications of interest. These specifics are determined by the system into which the array is inserted, in particular impedance matching of sources and loads.

First, to ensure a tunable oscillator, resonances in the junctions and arrays should be avoided by having minimal inductive and capacitive parasitics. This rules out long junctions and complex multidimensional arrays. Two methods of external frequency control can be used. (1) Use an *external feedback* loop, which taps off some of the oscillator power, mixes it down to a much lower frequency,

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TABLE I

We present the design values for a 18 GHz digital-analog converter and a 2 THz oscillator. We assume that  $I_c$  is 10 mA for the above cases.

Device	f (GHz)	$Z_L$ ( $\Omega$ )	n	$\Omega$	$V_c$ ( $\mu$ V)	R (m $\Omega$ )	N
J-DAC	18	50	2	1	37	3.7	13,433
J-Oscillator	2000	75	1	2	2,068	206.8	363

TABLE II

This table shows the constraints on junction spacing due to different substrates with different dielectric constants.

Device	Dielectric	$\epsilon_{\text{eff}}$	$\Lambda/4$ ( $\mu$ m)	Length/ JJ (nm)	Output
DAC	Si/Air	6.4	1647	123	1.00 V $\pm$
Oscillator	Quartz/Air	2.4	24	67	0.94 mW
Oscillator	Sapphire/Air	6.4	15	41	0.94 mW

compares it to an external reference, and adjusts the array bias. This method may require internal phase locking of the junctions or some form of high frequency feedback. In this method the array behaves as a variable frequency oscillator. The second method is to *subharmonically pump* the array at a lower frequency and bias the array so that it generates more than one quantized voltage pulse per drive cycle, i.e.  $f_0 = nf$ . The lower frequency is tunable and locked to an external frequency reference. In this method the array behaves as a frequency multiplier. This method does *not* require internal phase locking of the array and may work better for arrays with significant junction nonuniformity.

The output power of an oscillator will be determined by the application and by the impedance of the load. Generally, higher output power is desirable. The output power will be highest when the ac Josephson current is highest. The ac Josephson current is proportional to the junction critical current, which is maximized by increasing the junction dimensions to  $4\lambda_J$ . In the case of HTS junctions, the usual square geometry of the tunnel junction [3] is not appropriate, and an inline geometry should be used to calculate  $\lambda_J$  [4].

The junction characteristic frequency  $2e/hV_c$  should be chosen less than the desired operating frequency  $f_0$  to maximize the ac Josephson current in the fundamental frequency. However, phase locking will decrease as junction uniformity increases, in particular, as  $f_0 \gg f_c$  [5]. Thus the operating frequency should be in the range  $(1-3)f_c$ . For example, a 1-2 THz oscillator with a load impedance of 75  $\Omega$   $f_c = 1$  THz and  $I_c = 10$  mA, would have a junction resistance of about 200 m $\Omega$ . Similarly, a Josephson DAC driven at 18 GHz requires over 13,000 junctions. Some of these points are summarized in Table I.

The discussion to now has been a review of simple optimization concepts. We now turn to a brief discussion of the design criteria for lumped arrays fabricated on typical dielectrics. The following relationships are used in designing these electrically small arrays, and have been used to develop the values in Table II.

$$Z_{\text{array}} = NR_N \approx 50\Omega, \quad \Lambda = \frac{c}{f_0 \sqrt{\epsilon_R}}, \quad L_{\text{Array}} < \frac{1}{4} \Lambda.$$

The number of junctions N can now be chosen to match the array impedance to either a quasi-optical antenna or an on-chip detector. However, the maximum number of junctions is limited by requiring that the array remain a lumped element, that is, its total length is only 1/4 the length  $\Lambda$  corresponding to the maximum output frequency. Choosing an output frequency of 2 THz (150  $\mu$ m) and a 75  $\Omega$  quasi-optical antenna, the array length is limited to about 12  $\mu$ m for the necessary N= 375 junctions. Lumped arrays are preferred over distributed arrays for a number of reasons. Distributed arrays are intrinsically fixed frequency designs and their distributed nature increases the transmission line losses, which are particularly large at THz frequencies. Under the above assumptions, the junction spacing for the 375 junction lumped array is a challenging 32 nm. The array is tunable from 1-2 THz and delivers about 1 mW to the 75  $\Omega$  antenna at 2 THz. Smaller numbers of junctions (and output power) can be matched to antenna impedances as low as 25  $\Omega$  using junction spacings as large as 100 nm.

#### IV. HTS JOSEPHSON JUNCTIONS

In the past, we have explored several HTS junction technologies for arrays: SNS step-edge junctions, ramp-edge junctions, bicrystal junctions, and electron-beam irradiated

junctions. The e-beam junctions (EBJ) are excellent candidates because of their small size, allowing a large number of junctions to be placed in a small length [5]. Separations of 100 nm have been demonstrated, in the range discussed in the previous section. Because of this advantage, we are presently involved in a collaboration to develop electron-beam irradiated junction arrays. Figure 1(a) shows a schematic of the process and of a resulting lumped array.

Initial experiments in close spacing and in junction uniformity are presented in [5]. These results show promise for arrays numbering in the hundreds of junctions. Ultimately, very slow writing time may be the limiting factor in producing useful arrays by this technique. Long term stability must also be investigated.

A junction process that uses faster lithography than e-beam damage would be desirable for manufacturability.

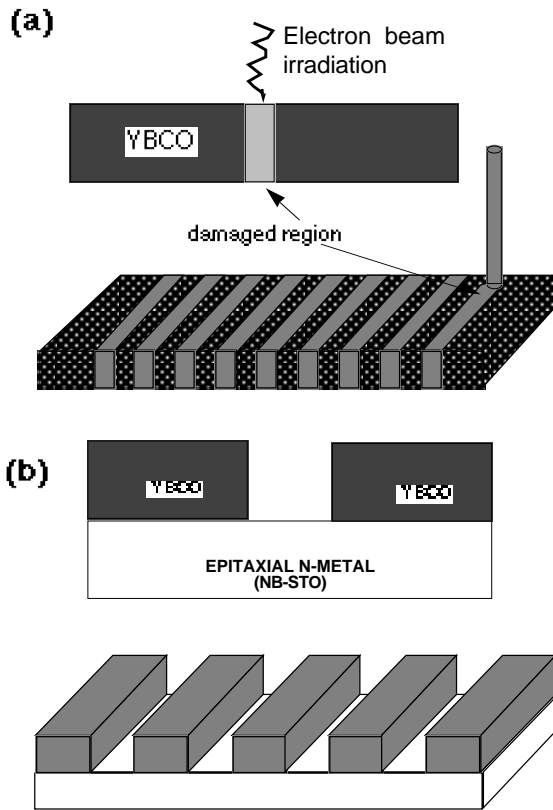


Fig.1 (a) Electron-beam irradiation damage forms a normal metal region in the YBCO. (b) E-beam lithography is used to form a bilayer microbridge SN-N-NS junction.

Resist-based e-beam lithography (EBL) will be investigated using epitaxial HTS/normal metal bilayers. As shown in Fig. 1(b), an epitaxial bilayer of YBCO on an oxide normal metal is patterned into a sequence of SNS microbridge structures. The etched pattern in the HTS layer is first formed by EBL and the resist pattern transferred by ion milling. A collaboration with the University of Colorado is presently underway to investigate Nb-doped SrTiO<sub>3</sub> (Nb-STO) as a normal metal. In this case, the important parameters we need to measure are the normal state properties of Nb-STO, in particular the normal metal coherence length over the temperature range of interest.

## V. SUMMARY

We have briefly reviewed the various individual junction characteristics needed for electrically small arrays. These lumped arrays may find significant use as precision digital-analog converters and THz oscillators if the formidable fabrication challenges are overcome, either in low or in high temperature junction systems.

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